

FIG. 2

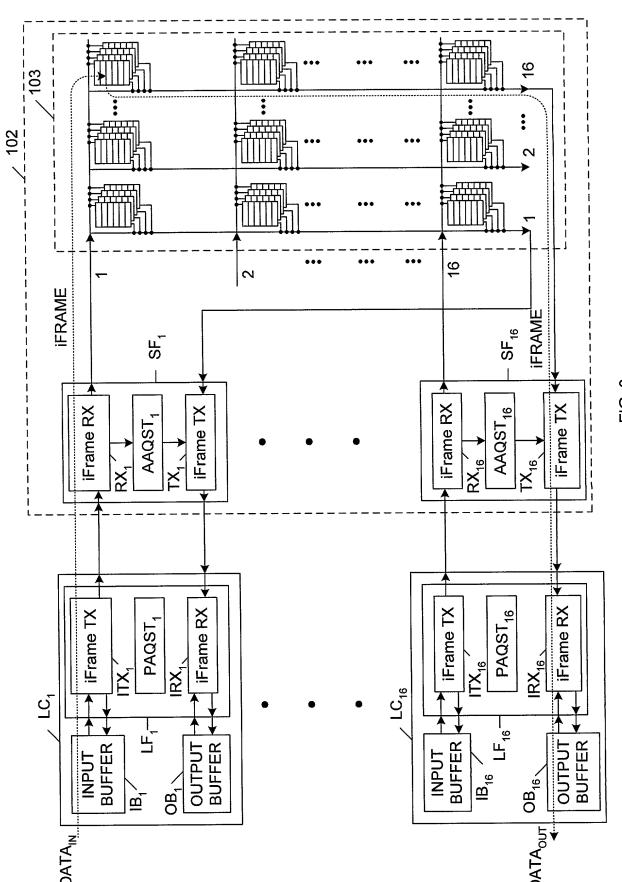


FIG. 3

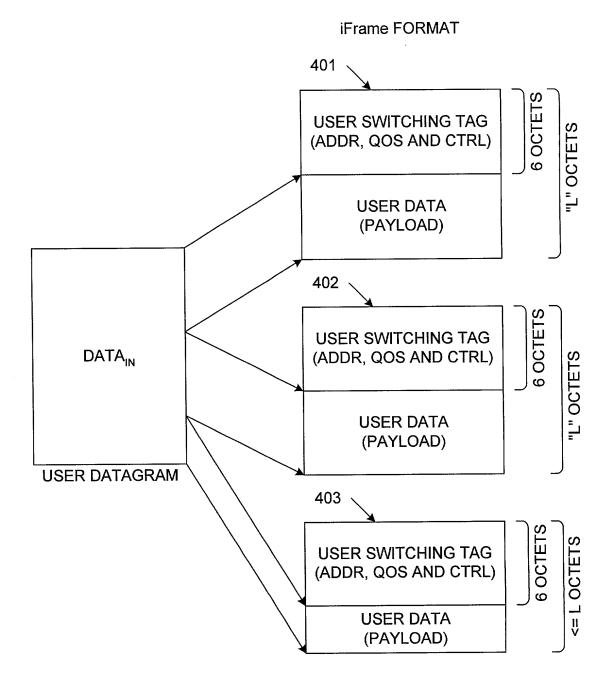


FIG. 4

501B \

#### INGRESS USER SWITCHING TAG FOR 501A \ **UNICAST IFRAMES** EGRESS PORT QoS E=0 F L C1 C2 M=0 (1-bit) (1-bit) (1-bit) (1-bit) (1-bit) (1-bit) (2-bit) **EGRESS SWITCH PORT ID** (8-bit) FLOW ID (8-bit) FLOW ID (8-bit) **FLOW ID** RESERVED = 00 (6-bit) (2-bit) TEC (CRC OR PARITY CHECK) (8-bit)

FIG. 5A

INGRESS USER SWITCHING TAG FOR

		MI	JLTI-CAS					
C1 (1-bit)	C2 (1-bit)	M=1 (1-bit)	E=0 (1-bit)	F (1-bit)	L (1-bit)	EGRESS PORT QOS (2-bit)		
	16-bit DIRECT MULTI-CAST EGRESS SWITCH PORT IDs (8-bit)							
	16-bit DIRECT MULTI-CAST EGRESS SWITCH PORT IDs (8-bit)							
14-bit MCID CONTINUED (8-bit)								
14-bit MCID CONTINUED RESERVED = 00 (6-bit) (2-bit)								
	TEC (CRC OR PARITY CHECK) (8-bit)							

# EGRESS USER SWITCHING TAG FOR UNICAST IFRAMES

601A				UNICAC	) I IFTAIVIE			
C1 (1-bit)	C2 (1-bit)	M=0 (1-bit)	E=0 (1-bit)	F (1-bit)	L (1-bit)	PQS UPDATE QOS (2-bit)		
	PQS UPDATE ID (8-bit)							
	22-bit FLOW ID (8-bit)							
	22-bit FLOW ID (8-bit)							
22-bit FLOW ID RESERVED = 0 (6-bit) (2-bit)								
	TEC (CRC OR PARITY CHECK) (8-bit)							

FIG. 6A

# EGRESS USER SWITCHING TAG FOR MULTI-CAST IFRAMES

601B				IVIOL 11-CA		VILO		
C1 (1-bit)	C2 (1-bit)	M=1 (1-bit)	E=0 (1-bit)	F (1-bit)	L (1-bit)	PQS UPDATE QOS (2-bit)		
	PQS UPDATE ID (8-bit)							
RESERVED = 0000 0000 (8-bits)								
14-bit MCID CONTINUED (8-bit)								
14-bit MCID CONTINUED RESERVED = 00 (6-bit) (2-bit)								
	TEC (CRC OR PARITY CHECK) (8-bit)							

#### **INGRESS AAQST** REQUEST 701A CONTROL iFrame C1=1 C2=1 **TYPE = 00** RESERVED=00 M=0 E=0 (1-bit) (1-bit) (2-bit) (1-bit) (1-bit) (2-bit) TEC (CRC OR PARITY CHECK) (8-bit)

FIG. 7A

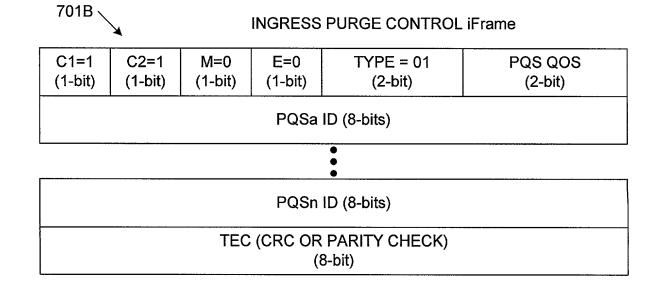


FIG. 7B

801A

### AAQST<sub>J</sub> TABLE UPDATE

C1=1 (1-bit)	C2=1 (1-bit)	M=0 (1-bit)	E=0 (1-bit)	F=0 (1-bit)	L=0 (1-bit)	TYPE=00 (2-bit)	
4-bit AC	QS <sub>J,1,1</sub> UP[	DATE INC	REMENT	4-bit A	4-bit AQS <sub>J,1,2</sub> UPDATE INCREMENT		
4-bit AC	QS <sub>J,1,3</sub> UP[	DATE INC	REMENT	4-bit A	4-bit AQS <sub>J,1,4</sub> UPDATE INCREMENT		
4-bit AC	QS <sub>J,2,1</sub> UP[	DATE INC	REMENT	4-bit A	4-bit AQS <sub>J,2,2</sub> UPDATE INCREMENT		
4-bit AQS <sub>J,2,3</sub> UPDATE INCREMENT				4-bit A	4-bit AQS <sub>J,2,4</sub> UPDATE INCREMENT		

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4-bit  $AQS_{J,15,1}$  UPDATE INCREMENT
4-bit  $AQS_{J,15,3}$  UPDATE INCREMENT
4-bit  $AQS_{J,15,3}$  UPDATE INCREMENT
4-bit  $AQS_{J,16,4}$  UPDATE INCREMENT

TEC (CRC OR PARITY CHECK) (8-bit)

801B <

# EGRESS PQS UPDATE CONTROL iFrame

	<u> </u>					
C1=1 (1-bit)	C2=1 (1-bit)	M=0 (1-bit)	E=0 (1-bit)	F=0 (1-bit)	L=0 (1-bit)	TYPE=01 (2-bit)
RESERVED = 00 (2-bits)		4-bit PO	QSa UPDA	PQSa QOS (2-bit)		
8-bit AQS/PQSa ID						

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RESERVED = 00 (2-bits)	PQSn QOS (2-bit)						
8-bit PQSn ID							
	TEC (CRC OR PARITY CHECK) (8-bit)						

FIG. 8B

